Please amend the second paragraph in page 11, as follows:

It is important that the vias in the adsubstrate align with the I/O pads on the chip, for at the next key step, the chips are attached to the adsubstrate to form a chip package, reference numeral (105), as shown in FIG. 2f such that the vias (170) reach the I/O pads. The attachment is achieved by subjecting the chip package to an assembly pressure between about 1.5 to 2.5 Megapascals (Mpa) and at the same time, to a temperature between about 250 to 350 °C. Next, the chip package assembly is encapsulated with a molding material (180), preferably, epoxy based resin to a thickness between about 100 to 500 μm, as shown in FIG. 2g. It will be obvious to those skilled in the art that other molding materials for electronics can also be used.

Please amend the first paragraph in page 12, as follows:

It is now a main feature of the present invention to perform ball mounting over the via openings of the adsubstrate, where the chip package is inverted such that the mounting material (190), preferably, solder is "balled" up as shown in FIG. 2h. It is further preferred that the solder (190) comprises tin-lead, or, tin-silver alloy. During continued process, solder flows to reach the I/O pads at the bottom of the vias, as shown in FIG. 2h. As a final step, the encapsulated chip package is die sawed to form the Chip Scale Package (CSP) of the present invention, as shown in FIG. 2i. FIG. 2j shows an alternate method of silk screening an adhesive material on to substrate (167) with holes corresponding to the AA I/O pads on the chip. That is, FIG. 2j is a top view of a portion of the patterned stencil where solid areas

(161) prevent the adhesive material (160) printing to the substrate (150) while open areas (163) allow the adhesive material (160) to print on the substrate (150), thus forming the adsubstrate (165) of FIG. 2e.

Please amend the last paragraph in page 13, as follows:

As a key aspect of the second embodiment, a substrate (370), similar to the BGA substrate (150) used in the first embodiment, is next prepared with drilled via openings (380) corresponding to the AA pad array on the CSPs to be attached as shown in FIG. 3c. It is preferred that substrate (370) comprises BT and has a thickness between about 150 to 300 μm. Then the CSP of FIG. 3b is die attached to substrate (370), as shown in FIG. 3d. This is accomplished at a pressure between about 1.5 to 2.5 Mpascals and temperature between about 250 to 350 °C. The resulting package is next encapsulated with a molding material (390) using a molding process as shown in FIG. 3e. This is followed by another key feature of the second embodiment, namely, a reflow ball mounting ~~(400)~~ process is performed to form a solder (400) over openings (360) and connected ~~that connect~~ to the AA I/O pads of the chip sites within the wafer, as shown in FIG. 3f. This is accomplished by forming solder (400) comprising tin-lead or tin-silver alloy.